Test Report V1.0
Single Event Effects (SEE) Testing of the
MB85R256 Ferroelectric Random Access Memory (FRAM)

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I. Introduction

The MB85R256 is an FRAM chip in a configuration of 32,768 words x 8 bits, using the ferroelectric process and silicon gate CMOS process technologies for forming the nonvolatile memory cells. Unlike SRAM, the MB85R256 is able to retain data without back-up battery. The memory cells used for the MB85R256 have improved at least 10^{10} times of read/write access per bit, significantly outperforming FLASH memory and EEPROM in durability. The MB85R256 uses a pseudo - SRAM interface compatible with conventional asynchronous SRAM.

II. Tested Devices

The FRAM devices were designed and fabricated by Fujitsu Semiconductor. All devices were characterized prior to exposure, ensuring proper operation. The two devices tested are from the 0405 Lot Date Code (LDC). Complete package markings for these devices are:

F JAPAN
MB85R256
0405 M26

These are 28 pin devices in a SOP package.

Product data sheet:
http://edevice.fujitsu.com/fj/DATASHEET/e-ds/e513101.pdf

III. Test Facility Information

Facility:
Texas A&M University Cyclotron Single Event Effects Test Facility, using the 15 MeV/amu tune

Total Beam Time:
8 hours

Maximum Fluence for one run:
1E6 p/cm^2

Flux used:
1E3 p/cm^2/s to 7E4 p/cm^2/s as appropriate

Ions used	LET (MeVcm^2/mg)
Ne	2.8
Ar	8.9
Cu	21.3
Kr	30.1
Cu at 45 angle	42.6

IV. Test Methods

Temperature:
Room temperature

Test Voltage:
Nominal (3.3 Volts)

Test Hardware:
The Low Cost Digital Tester (LCDT) was used to perform this testing. Each device under test (DUT) was socketed on a daughter card with the appropriate VHDL written to the LCDT in order to perform the required SEE testing as detailed below. Appropriate power supplies were used with DUT current strip charted and monitored for over current conditions. Shown below is the test setup at TAMU (Figure 1).

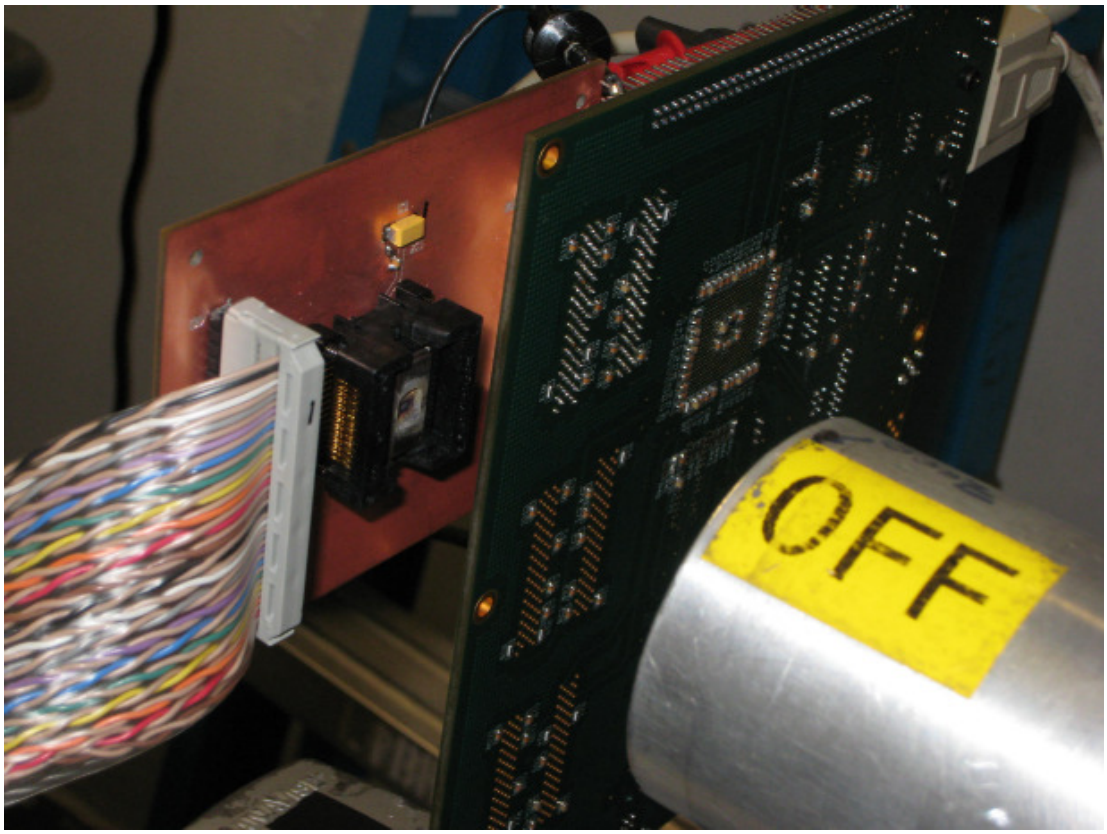

Figure 1: Photograph of FRAM Test Setup

V. Test Results

Test Procedures:

At each LET value, testing began with a static test using an all zero's, then all one's pattern. No more than 10% of the memory cells upset during any one run. For all tests, static and dynamic modes were run, showing similar results for onset of a latch-up event's LET threshold. Normal operating current while in dynamic mode was under 4mA.

Testing of the FRAM began at a flux of 1E4 p/cm^2/s until a fluence of 1E6 p/cm^2 was achieved with no errors or latch-up occurring. Neon and Argon ion beams both showed similar results and the flux was increased to 7E4 p/cm^2/s to achieve the same fluence in a shorter period of time.

When the ion was changed to Cu at a LET of 21.3 MeVcm^2/mg latch-up events occurred for some runs as well as a few errors, at most 3 errors in one run. After testing 21.3 MeVcm^2/mg was found to be the closest value of the parts LET threshold to latch-up events. When the ion was changed to Krypton, latch-up occurred in all tests, with very

few recorded errors, at most 1 error in one run. This being said, the most notable data is the relation of fluence until latch-up, shown in Figure 2 below.

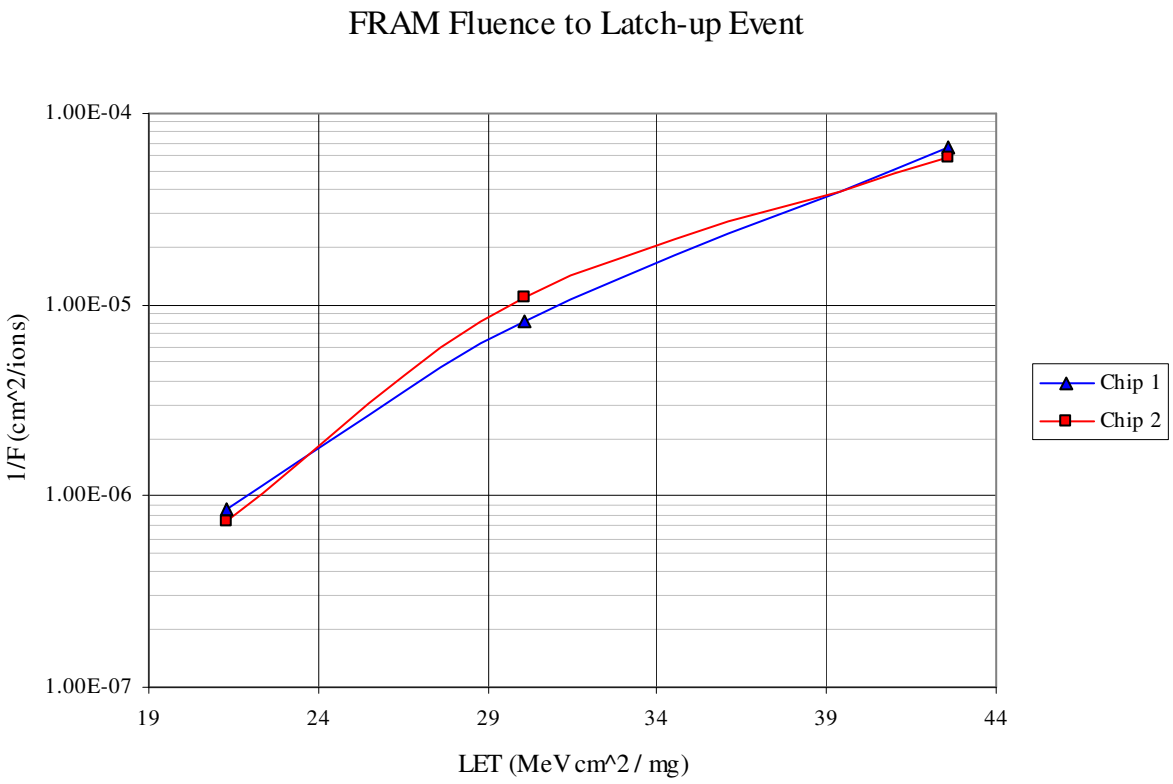

Figure 2: MB85R256 FRAM Fluence to Latch up for three values of LET

Both of the tested chips had statistically similar results for onset of latch-up events and similar responses to higher LET with lower flux rates. Plotted in Figure 2 is the average fluence to latch-up, with at a minimum of 5 test runs on each chip, at each LET. It should be noted that at the LET of 30.1 MeVcm^2/mg there was a very broad range of fluence that lead to the latch-up event. More testing would show susceptibility to lower fluence, at higher LET if the flux were significantly reduced. However, testing was stopped due to time restriction and to avoid total dose effects on the two parts being tested.

Test Requirements Met:

1. Testing was conducted at 3.3 Volts
2. FRAM test pattern was controllable to settings of all zeros, all ones, checkerboard and reverse checkerboard patterns.
3. Testing was performed in both a static and dynamic mode. In the static test the device memory was written and verified, exposed without being exercised, and then the device was read, with errors corrected. All errors and error memory locations were recorded after static runs. The device memory is to be read at least three times after exposure to verify that there are no stuck bits. In the dynamic

test the device memory was written and verified, the device was then placed into read/write/correct mode for at least three cycles of the memory (to ensure the device is performing correctly prior to exposure). The device was then exposed while being exercised, recording all errors, error memory locations, and timestamp.

4. Testing was done across the Linear Energy Transfer (LET) range from threshold 2.8 MeV-cm^2/mg through 42.6 MeV-cm^2/mg, over a statistically significant number of runs.

Test Requirements Not Met:

1. Time restricted data being taken at high (3.6V) and low (3.0V) voltages.
2. Testing was not done up to a LET of 47.3 MeV-cm^2/mg, (Xenon at normal incidence) latch-up occurred to early in the test to go that high in LET, even with reduced flux values.